

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	532	(257/324,326).CCLS.	USPAT; US-PGPUB	2003/07/21 14:46
2	BRS	L2	50	1 and @pd>20030115	USPAT; US-PGPUB	2003/07/21 14:46
3	BRS	L5	105	("3895360" "4016588" "4017888" "4151021" "4173766" "4173791" "4257832" "4306353" "4342149" "4360900" "4380057" "4471373" "4521796" "4527257" "4586163" "4630085" "4667217" "4742491" "4769340" "4780424" "4847808" "4870470" "4941028" "5021999" "5042009" "5075245" "5104819" "5159570" "5168334" "5172338" "5175120" "5214303" "5260593" "5293563" "5295108" "5305262" "5311049" "5324675" "5338954" "5345425" "5349221" "5350710" "5359554" "5375094" "5393701" "5394355" "5412601" "5414693" "5418176" "5418743" "5422844" "5424567" "5424978" "5426605" "5434825" "5436481" "5440505" "5450341" "5450354" "5455793" "5467308" "5477499" "5496753" "5518942" "5523251" "5553018" "5563823" "5592417" "5599727" "5606523" "5654568" "5656513" "5712814" "5726946" "5751037" "5754475" "5760445" "5768192" "5787036" "5793079" "5801076" "5812449" "5825686" "5836772" "5841700" "5847441" "5864164" "5870335" "5886927" "5903031" "5946558" "5963412" "5973373" "5991202" "6018186" "6020241"	USPAT	2003/07/21 14:54

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 5424978 A	15	Non-volatile semiconductor memory cell capable of storing more than two different data and method of using the same	365/184	365/185.03; 365/185.19	Wada, Toshio et al.
2	US 5434825 A	17	Flash EEPROM system cell array with more than two storage states per memory cell	365/185.2 4	257/E21.179; 257/E21.68; 257/E27.103; 257/E29.302; 257/E29.306; 365/182; 365/185.29; 365/189.07; 365/218	Harari, Eliyahou
3	US 5440505 A	21	Method and circuitry for storing discrete amounts of charge in a single memory element	365/45	365/185.03; 365/185.22; 365/189.01; 365/218; 365/230.01	Fazio, Albert et al.
4	US 5450341 A	31	Non-volatile semiconductor memory device having memory cells, each for at least three different data writable thereinto selectively and a method of using the same	365/185.2 4	365/184; 365/218	Sawada, Kikuzo et al.
5	US 5754475 A	12	Bit line discharge method for reading a multiple bits-per-cell flash EEPROM	365/185.2 5	365/185.2	Bill, Colin et al.
6	US 6552387 B1	29	Non-volatile electrically erasable and programmable semiconductor memory cell utilizing asymmetrical charge trapping	257/324	365/185.33	Eitan, Boaz